TRF3703 Quadrature Modulator Evaluation Module

User's Guide

Literature Number: SLWU042B
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TRF3703 Quadrature Modulator Evaluation Module

1 Overview

This document relates to the TRF3703-33 and TRF3703-15 (hereinafter referred to as TRF3703) direct quadrature modulator for applications in the transmit path of base stations and communications equipment. The TRF3703 operates between 400 MHz and 4 GHz. The quadrature modulator is used for upconversion of signals from the transmit chain DAC to the RF power amplifier device. Evaluating modulator complex performance involves careful bias-voltage setup, an LO signal, and two differential (I/Q) signals at the input of the modulator. This document describes the wide range of test options available and the factors that must be considered in using this EVM.

1.1 Purpose

The TRF3703 evaluation module (EVM) is intended for the evaluation of the TRF3703-33 and TRF3703-15 direct-launch quadrature modulators. Unless otherwise stated, the functionality described in this manual applies to both the TRF3703-33 and TRF3703-15 devices.

1.2 EVM Circuit Overview

The EVM comes configured for differential I/Q input signals via four SMA connectors as shown in the schematic, Figure 14, and in Table 1.

For the upper sideband, the I signals are connected to J4 (I+) and J3 (I–). The Q signals are connected to J5 (Q–) and J6 (Q+). The LO signal is fed to SAM connector J1, whereas J2 must be terminated with 50 Ω to ground. SMA connector J7 is used to monitor the RF output signal from the quadrature modulator (U1).

The quadrature modulator requires a supply voltage of 4.5 V–5.5V at 235 mA from a regulated power supply through headers W1 and W2. The TRF3703-33 requires a 235-mA current limit, whereas the TRF3703-15 requires 205 mA.

The TRF3703-33 and TRF3703-15 quadrature modulators require a dc common-mode bias voltage (3.3 VDC and 1.5 VDC, respectively) on all four input pins.

1.3 Power Requirements

The TRF3703 EVM requires two 5-V V_{CC} dc power-supply connectors through headers W1 and W2. Header W1 supplies 5 V to the LO circuitry, and W2 supplies 5 V to the modulator circuitry.

CAUTION

Voltage Limits

Exceeding 5.6 V may damage the TRF3703.

1.4 TRF3703 EVM Operating Procedure

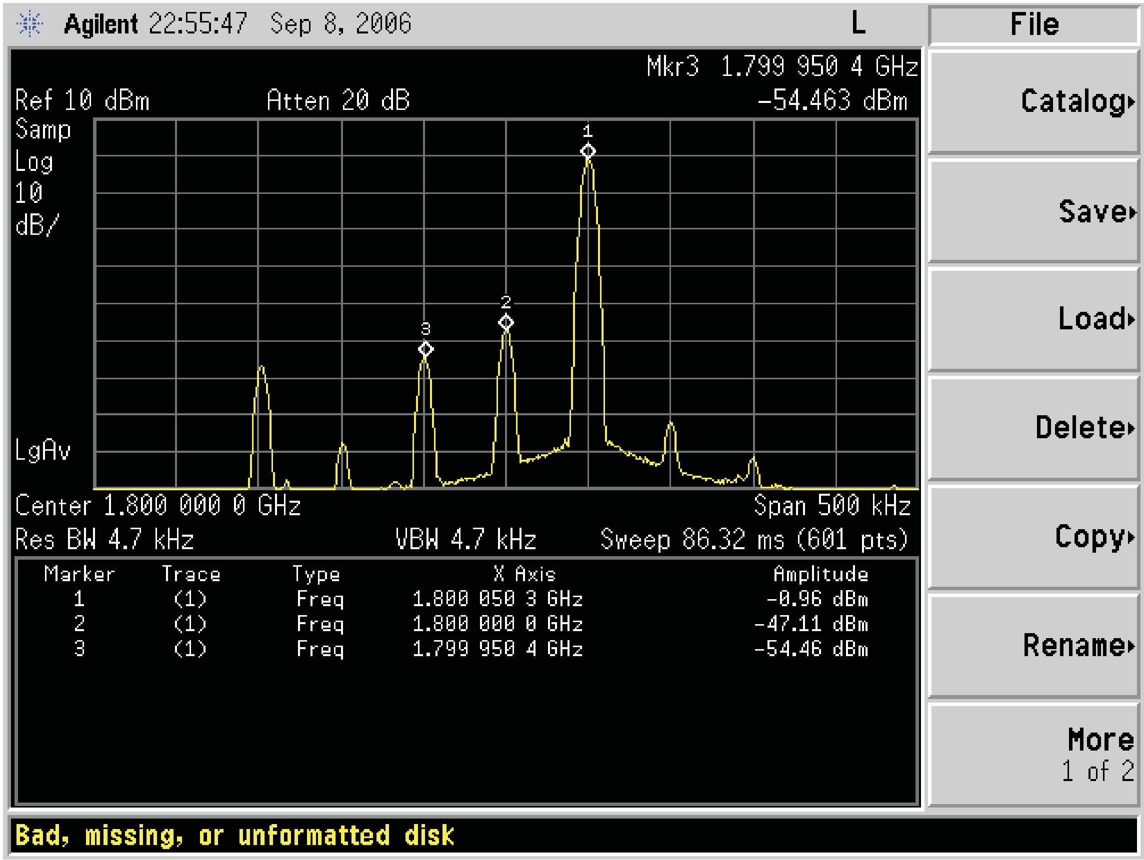
Set up the EVM as follows:

1. Power-supply connection:
   a. Switch on the V_{CC} (5-V) supply and set the current limit set to 235 mA.
   b. Connect the 5-V supply to headers W1 and W2.
   c. Verify that the current drawn is approximately ≤ 205 mA for the TRF3703-15 and ≤ 235 mA for the TRF3703-33.
2. Use a suitable 50-Ω output signal generator (LO = ±5 dBm) or the TRF3761 to supply the LO signal at desired frequency to J1, and terminate J2 with 50 Ω to ground.
3. Use a DAC or an arbitrary waveform generator to provide the I/Q input signals. A typical setup is as follows: a 1-Vp-p sine wave, a frequency of 50 KHz, a dc-offset of 0 V, and an output impedance of 50 Ω (typically an ESG vector signal generator or similar).
4. Set the common mode on the ESG to either 1.65 V or 0.75 V, depending on device type (set to 1.65 V for the TRF3703-33, set to 0.75 V for the TRF3703-15).
5. Use an arbitrary waveform generator to suppress the sideband. Adjust the I/Q amplitude and phase of the CW signal coming from the arbitrary waveform generator.
6. Connect a spectrum analyzer to the SMA connector marked RFOUT (J7) and monitor the TRF3703 output.

1.4.1 Typical Test Results

1.4.1.1 Un-Optimized Sideband Suppression

measures the amount by which the unwanted sideband of the input signal is attenuated in the output of the modulator, relative to the wanted sideband. This assumes that the baseband inputs delivered to the modulator input pins are perfectly matched in amplitude and are exactly 90° out of phase. Un-optimized sideband suppression is measured in dBc. An iterative test is required in order to match perfectly the inputs to the modulator. This ensures that any equipment, board, or signal conditioning component imbalances are corrected before the signals are applied to the device under test. Once the baseband inputs to the modulator are balanced, the amount of suppression attained is a measure of the internal mismatches of the modulator, inherent to any modulator design. This suppression is the one specified in the TRF3703 datasheet. See Figure 1.

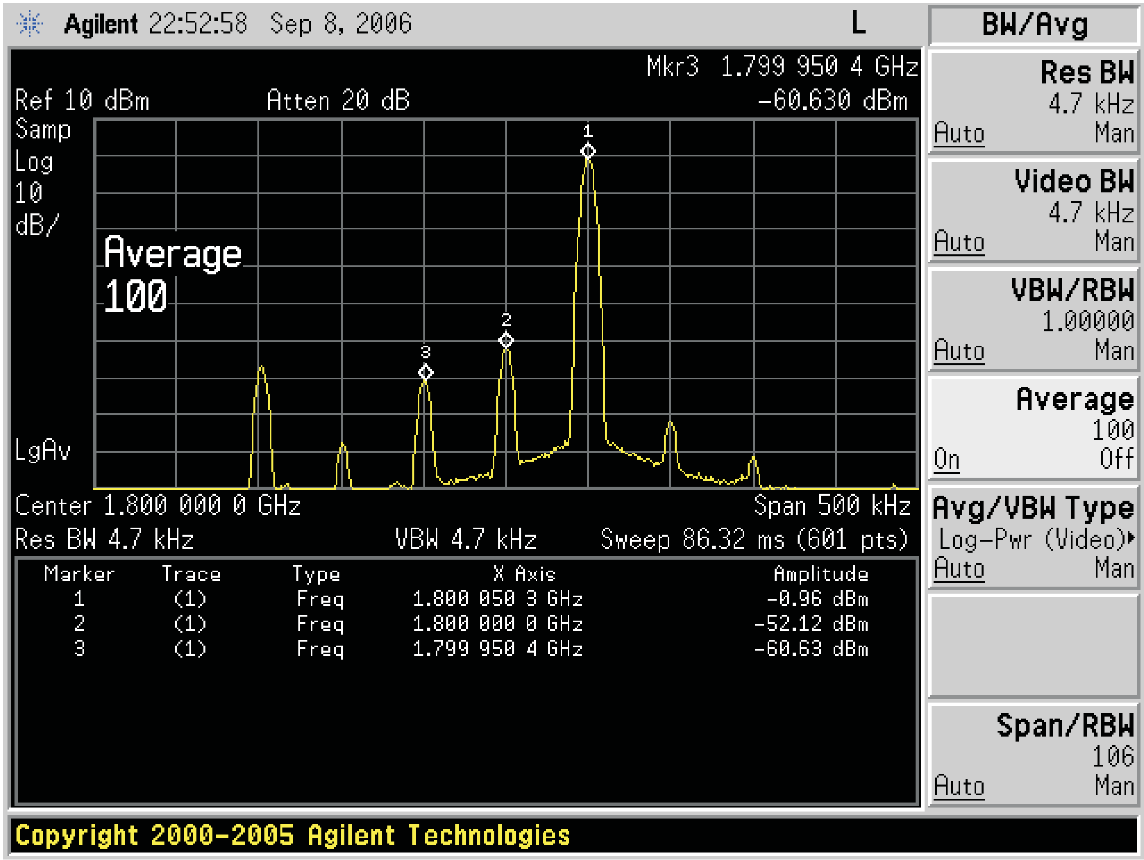


C003

Figure 1. Un-Optimized Sideband Suppression

1.4.1.2 Optimized Sideband Suppression

There are two ways to change the sideband suppression of the TRF3703. One is the amplitude between the four inputs, and the second is the phase of the four inputs. The ideal condition is when all four inputs (I, $\overline{I}$, Q, and $\overline{Q}$) have exactly the same amplitude and the phase relationship is: I = 0°, $\overline{I}$ = 180°, Q = 90°, and $\overline{Q}$ = 270°. Also, the optimization of the sideband is controlled by the amplitude and phase of the I and Q signals, which are controlled with the gain settings of the DAC. This is an iterative procedure that results in optimized suppression levels that exceeds 60 dBc. The level of suppression observed depends on the amount of resolution available from the DAC driving the modulator. By using TI's DAC568X, the user can take advantage of built-in features (DAC fine gain) to optimize the sideband suppression by changing the amplitude relationship of the signals. If another DAC is used, then the user must provide this level of adjustment by controlling the regular digital inputs to the DAC. See Figure 2.



C002

Figure 2. Optimized Sideband Suppression

1.4.1.3 Carrier Feedthrough

Carrier feedthrough is the amount of the LO that leaks onto the output spectrum of the modulator. Ideally for the TRF3703, inputs (I, $\overline{I}$, Q, and $\overline{Q}$) must be at approximately 3.3 V for TRF3703-33 and 1.5 V for TRF3703-15. The DAC dc settings are also useful to correct the dc mismatch between I and $\overline{I}$ and between Q and $\overline{Q}$ to correct for the LO feedthrough. If using TI's DAC568X, then the internal controls for the IQ offsets provide excellent carrier suppression (very low LO leakage). Alternatively, if an ESG is being used, adjust the I and Q voltage offsets in mV steps until you obtain the minimum carrier feedthrough. A typical carrier feedthrough value exceeds 50 dBm. See Figure 2.

1.4.1.4 GSM (EDGE EVM Measurements)

1. Provide a GSM edge signal of the desired frequency into the differential baseband inputs (example sample rate = 4.33 MHz).
2. Use a spectrum analyzer with edge personality to measure the transmit power to either 0 or –5 dBm.
3. PSA: Mode → GSM(w/ EDGE) → measure → Transmit Pwr(usually 0 or –5 dBm) → more → EDGE EVM.
4. ESG: Mode setup → select waveform → highlight EDGE → select waveform → ARB setup → type 4.33333 MHz → I/Q → I/Q output control → Common mode I/Q offset → (set to either 1.65 V for TRF3703-33 or to 0.75 V for TRF3703-15) → I/Q → I/Q output control → I/Q output atten (adjust to get desired transmit power to either 0 or –5 dBm).

See Figure 3.

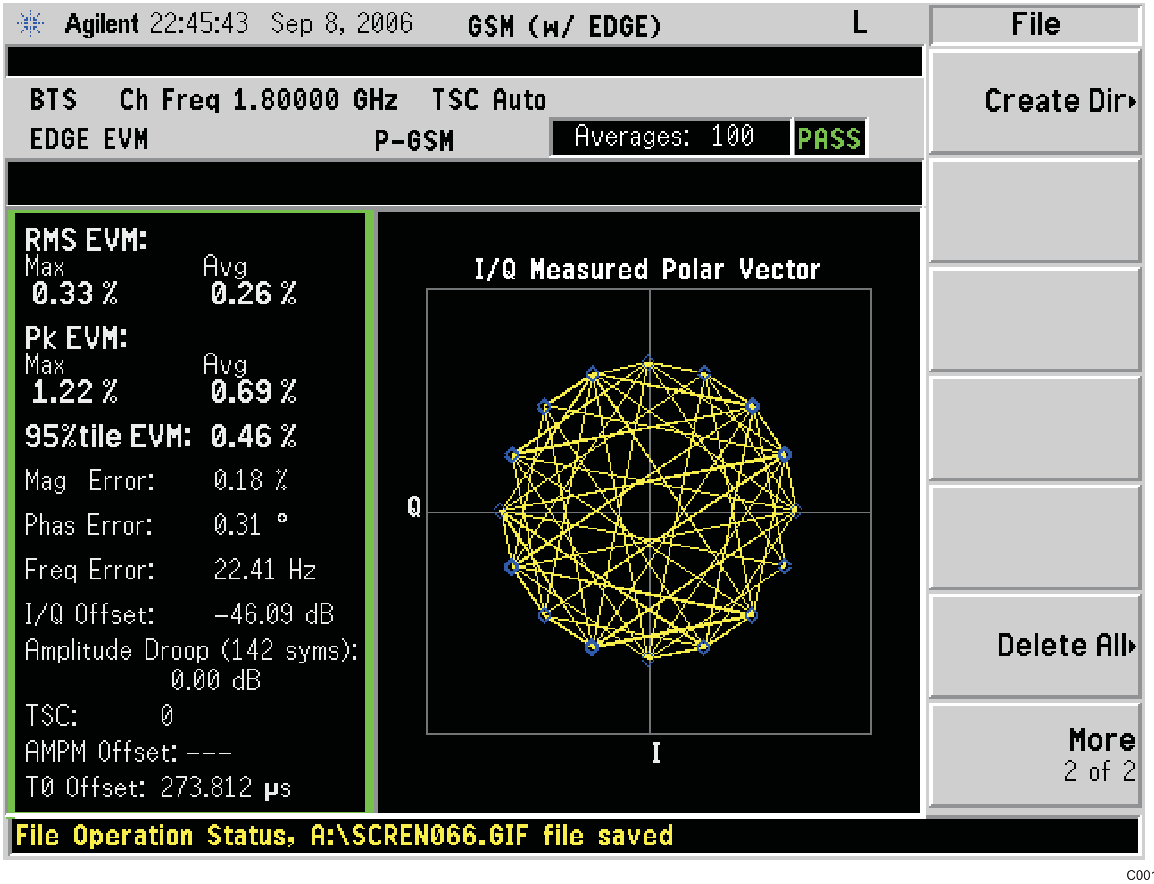
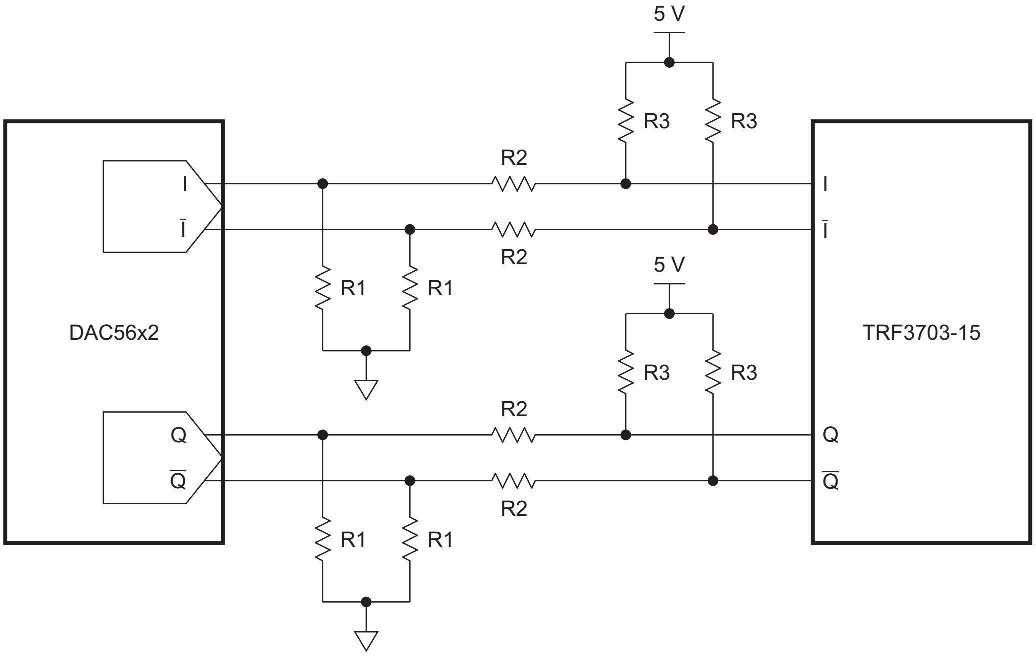


Figure 3. GSM EDGE EVM at 1800 MHz

1.4.2 Interface to TI's DAC

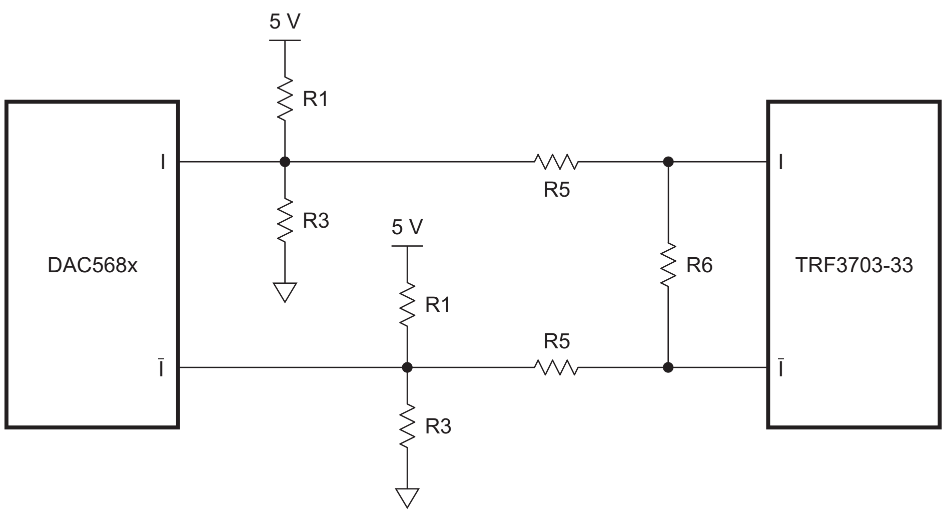
Both the TRF3703-33 and the TRF3703-15 work well with TI's DACs. The TRF3703-33 is well suited to work with TI's DAC568X family, and the TRF3703-15 is well suited to work with TI's DAC56X2 series. Each DAC series is optimized to work at certain common-mode voltage. The DAC568X has a common-mode of 3.3 V, while the DAC56X2 has a 0.7-V common-mode voltage. Figure 1 shows an interface network to interface both DAC series to the TRF3703.



TYPICAL VALUES		
R1	**R2**	**R3**
53 Ω	210 Ω	931 Ω

NOTE: A DAC interface calculator is available (SLWC083).

Figure 4. 1.5-V Interface Network for 19.2 mA Full Scale



LOSS		1 dB	2 dB	3 dB	4 dB	5 dB
Pullup	R1	115	115	115	115	115
Pulldown	R3	634	634	634	634	634
Series	R5	11	21	30	37.4	45.3
Shunt	R6	187	165	147	130	118

Figure 5. 3.3-V Interface Network for 19.2 mA Full Scale

2 Physical Description

This chapter discusses the four-layer PCB layout, component placement, and list of components used on the evaluation module.

2.1 PCB Layout

The EVM is constructed on a four-layer, 38,1-mm × 38,1-mm × 1,579-mm thick PCB using FR-4 material. Figure 6 through Figure 12 show the individual layers.

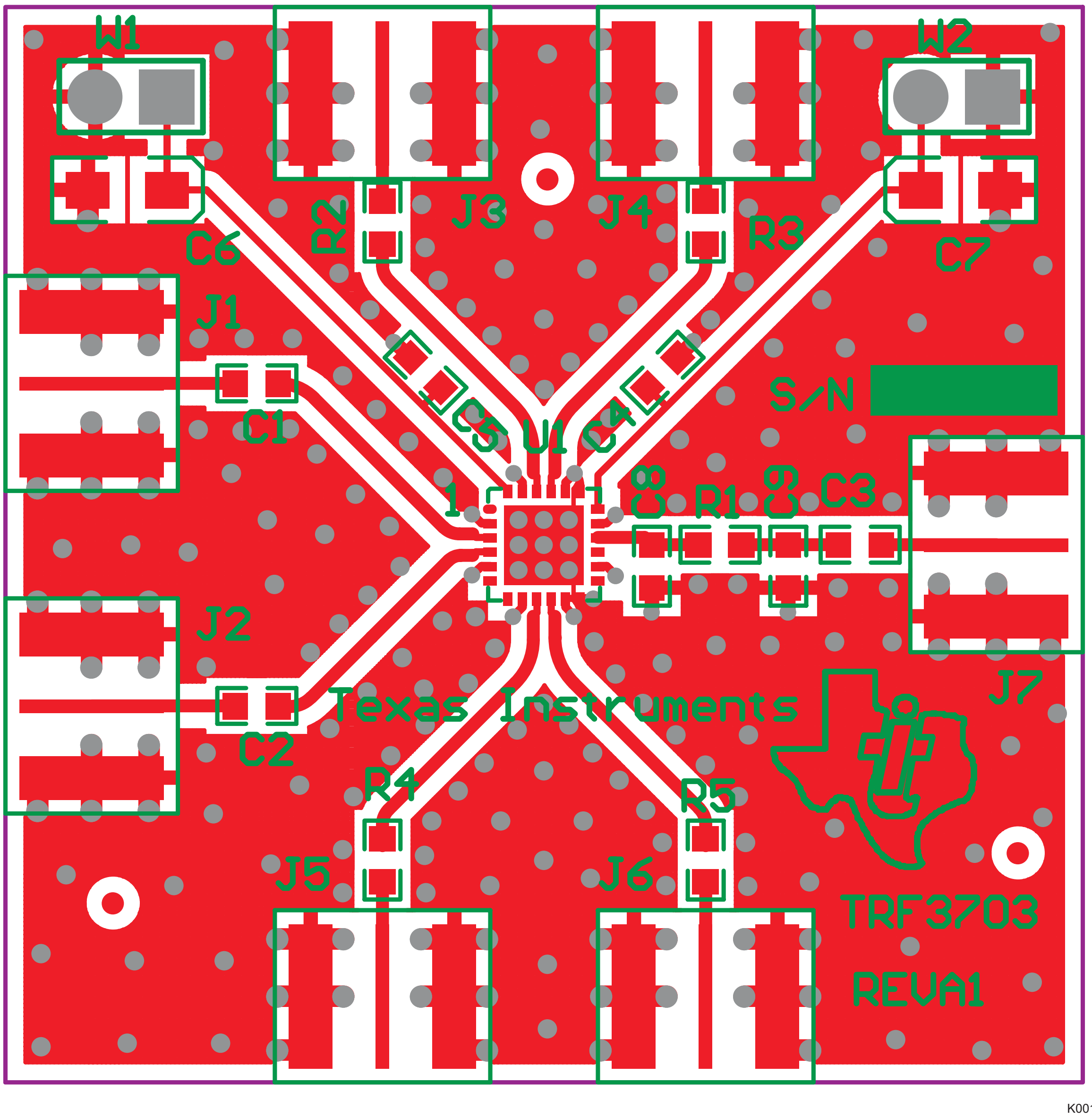


Figure 6. Top Layer

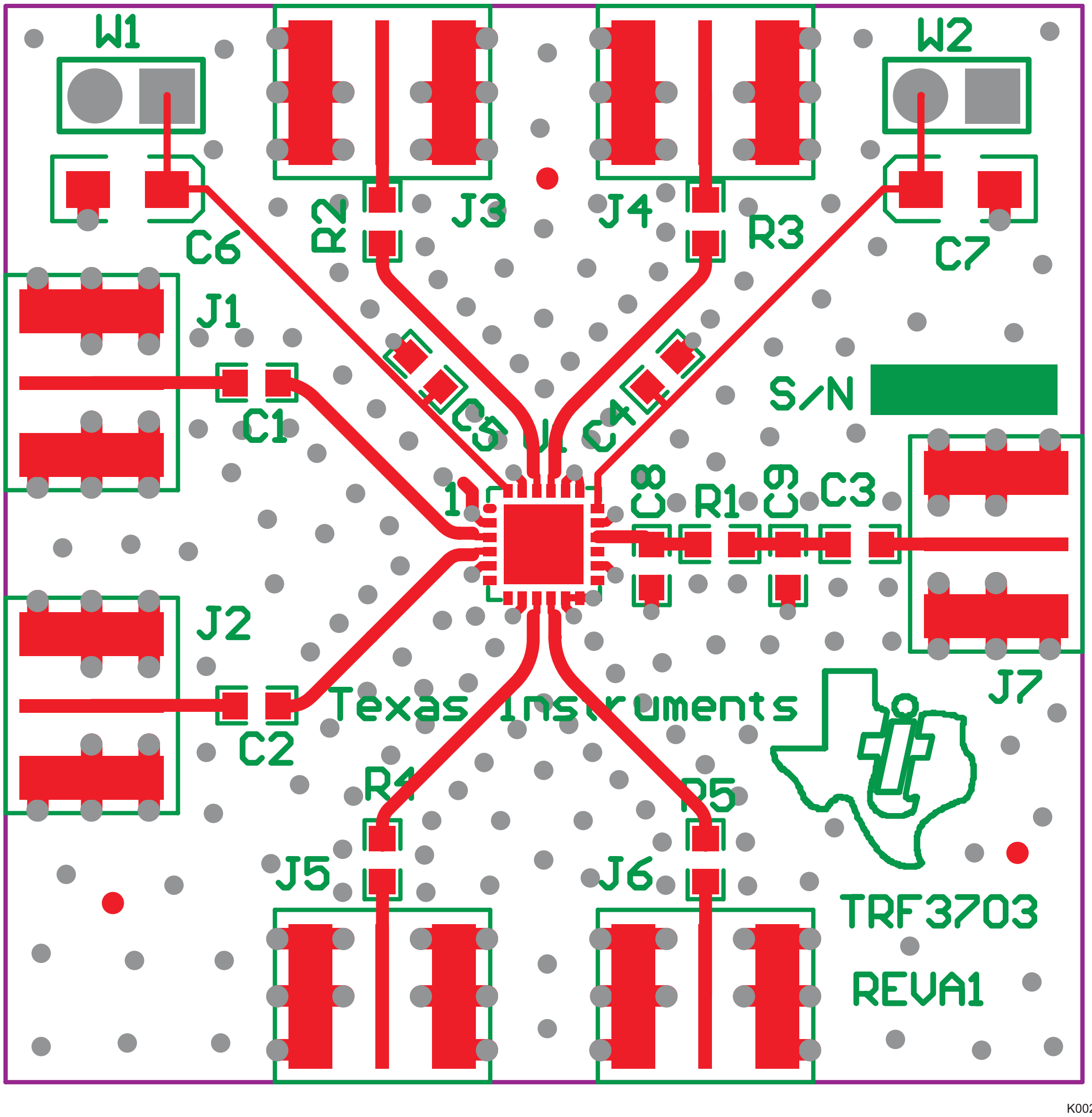


Figure 7. Top Layer–NH

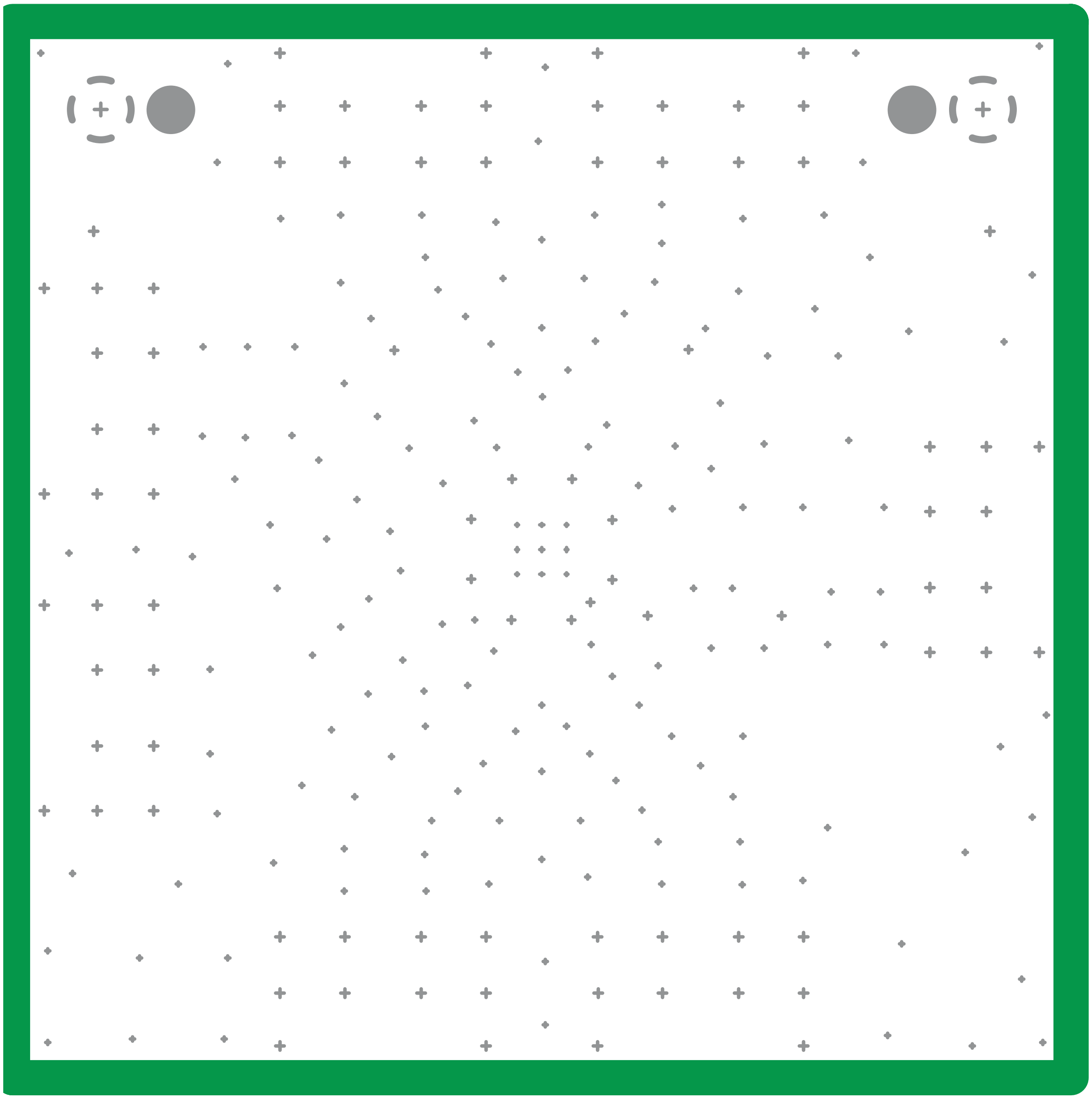


Figure 8. Ground Plane L2

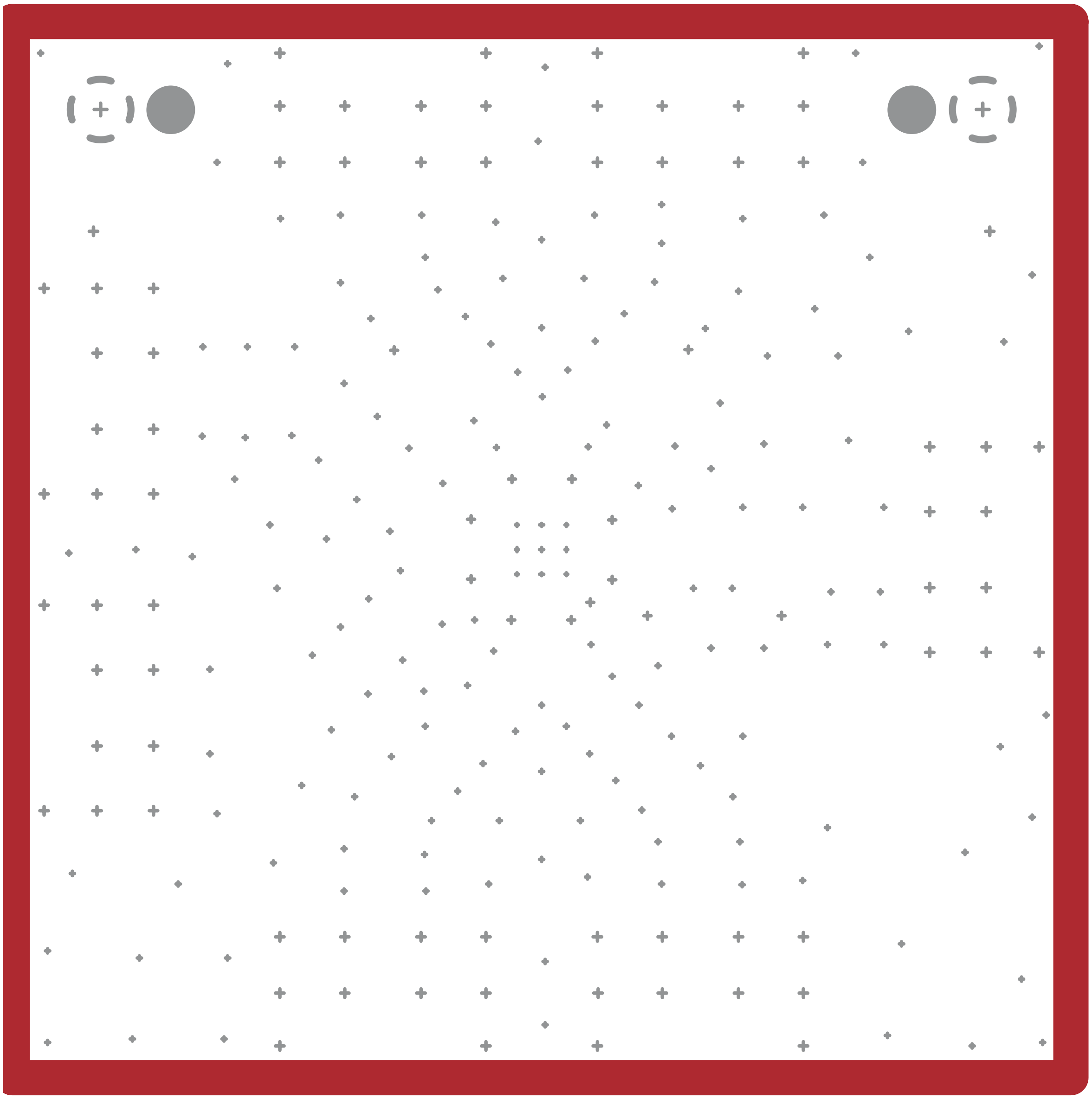


Figure 9. Ground Plane L3

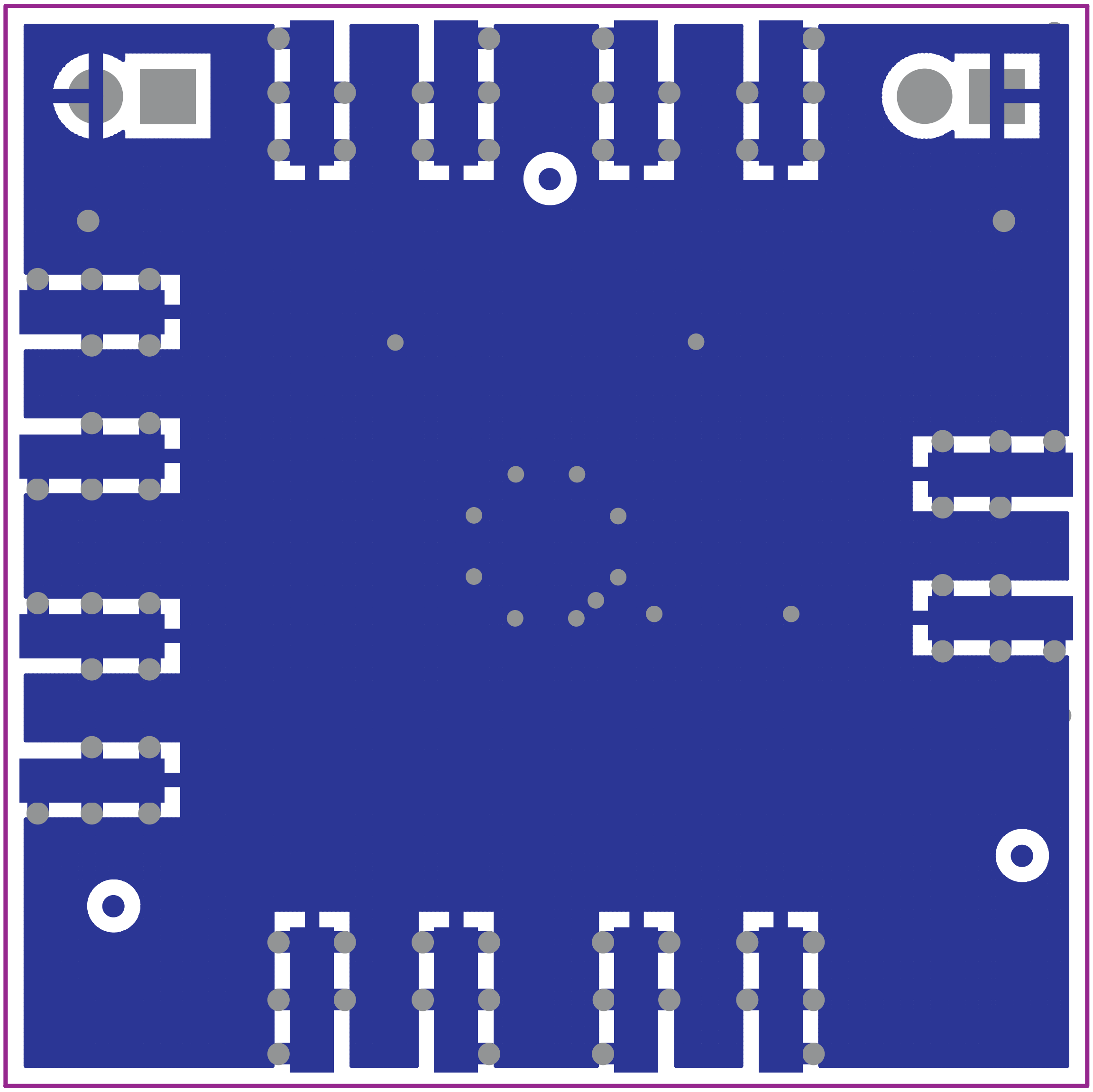


Figure 10. Layer 4—Bottom Layer

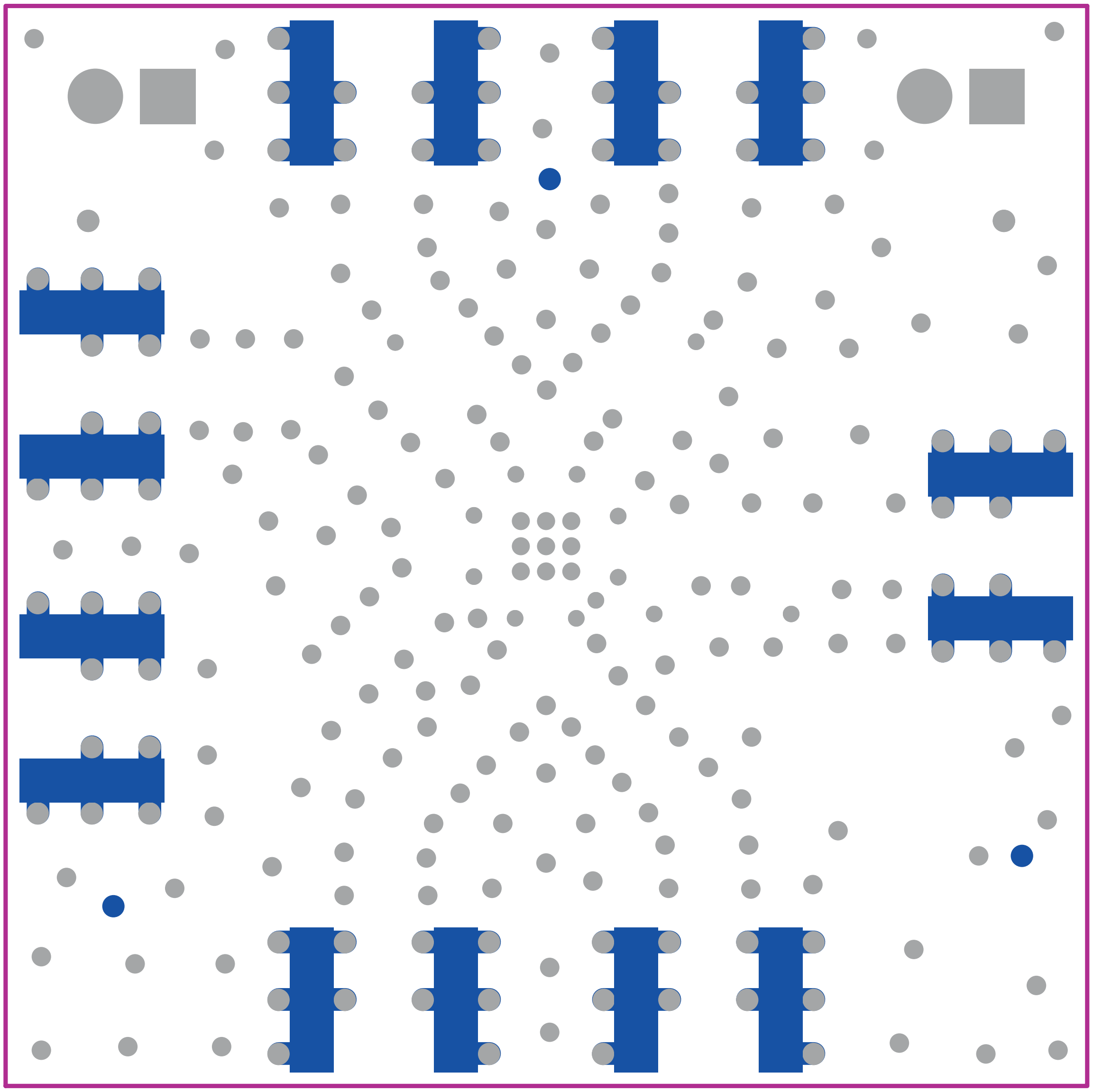
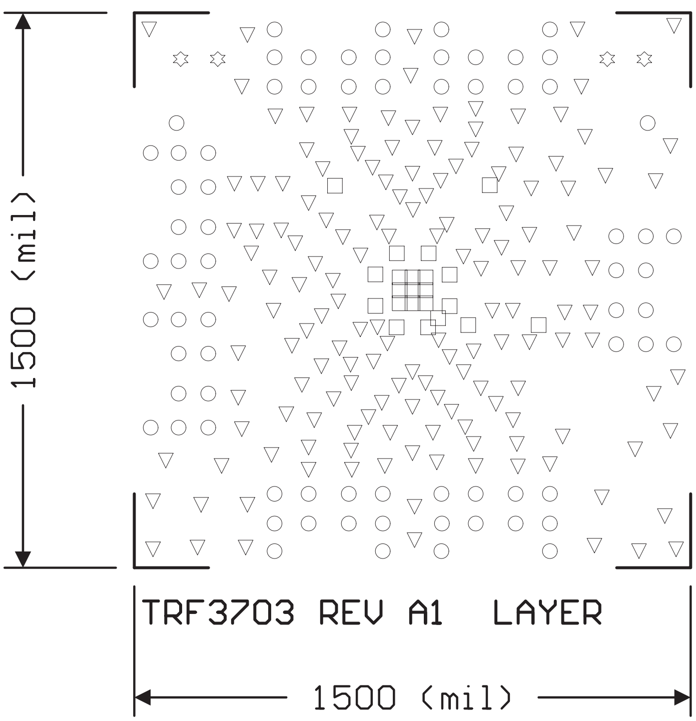


Figure 11. Layer 4—Bottom Layer–NH

Notes:

1. PWB TO BE FABRICATED TO MEET OR EXCEED IPC–6012, CLASS 3 STANDARDS AND WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 3 - CURRENT REVISIONS
2. BOARD MATERIAL AND CONSTRUCTION TO BE UL APPROVED AND MARKED ON THE FINISHED BOARD.
3. LAMINATE MATERIAL: POLYCAD 370 TURBO/HR
4. COPPER WEIGHT: 1oz FINISHED
5. FINISHED THICKNESS: .062 +/– .010. TOP METAL TO GND PLANE DIELECTRIC THICKNESS TO BE 10 MIL +/- .5 MIL
6. MIN PLATING THICKNESS IN THROUGH HOLES: .001"
7. GOLD FINISH, 50–100 MICRO OF NICKEL
8. LPI SOLDERMASK BOTH SIDES USING APPROPRIATE LAYER ARTWORK: COLOR = GREEN
9. LPI SILKSCREEN AS REQUIRED: COLOR – WHITE
10. VENDER INFORMATION TO BE INCORPORATED ON BACK SIDE WHENEVER POSSIBLE
11. MINIMUM COPPER CONDUCTOR WIDTH IS: 10 MILS MINIMUM CONDUCTOR SPACING IS: 5 MILS
13. TOP LAYER 18 MIL TRACES ARE CONTROLLED IMPEDANCE, 50 OHM LINES.



TRF3703 BOARD STACKUP	
TOP LAYER	1.2
370 TURBO	10.0
GND PLANE 1	1.2
TBD	37.2
GND PLANE 2	1.2
370 TURBO	10.0
BOTTOM LAYER	1.2

□	22	10 mil	0.254 mm	PTH
○	72	12 mil	0.3048 mm	PTH
▽	156	13 mil	0.3302 mm	PTH
✡	4	37 mil	0.9398 mm	PTH
	254	Total		

D001

Figure 12. Drill Pattern

2.2 Parts List

Table 1. Bill of Materials for TRF3703 EVM

Value	Footprint	QTY	Part Number	Vendor	Digi-Key Number	REF DES	Not Installed
Tantalum 4.7-µF, 10-V, 10% capacitor	3216	2	T491A475K010AS	KEMET	399-1561-1-ND	C6, C7	
1000-pF, 50-V, 5% capacitor	603	2	ECJ-1VC1H102J	Panasonic	PCC2151CT-ND	C4, C5	
100-pF, 50-V, 5% capacitor	603	3	ECJ-1VC1H101J	Panasonic	PCC101ACVCT-ND	C1, C2, C3	
Capacitor	603	0					C8, C9
0-Ω resistor, 1/10-W, 5%	603	5	ERJ-3GEY0R00V	Panasonic	P0.0GCT-ND	R1, R2, R3, R4, R5	
TRF3703	24-QFN-PP-4X4MM	1		TI		U1	
SMA connectors	SMA_END_SMALL	6	16F3627	Newark	142-0711-821	J1, J2, J3, J4, J5, J6, J7	
2POS_HEADER	2POS_JUMP	2	HTSW-150-07-L-S	SAMTEC	N/A	W1, W2	

3 Circuit Description

This chapter discusses the various functions of the EVM.

3.1 Circuit Function

- Headers W1 and W2 supply 5-V V_{CC} dc power to the modulator. Header W1 supplies 5 V to the LO circuitry, and W2 supplies 5 V to the modulator circuitry.
- Four SMA connectors are provided on the EVM for inputting differential I/Q signals directly to the input pins of the TRF3703. Connectors J3, J4, J5, and J6 are used to connect the signal source I/Q signals directly to the TRF3703.
- Two SMA connectors are provided for LO input: J1 = LOP and J2 = LON. Terminate whichever LO port is not being used through 50 Ω to ground.
- One SMA connector is for RF_OUT: J7.

3.1.1 Power

Table 2. Power Supply J1

J1 Pin	Description
W1	5-V (V_{CC}), U1 analog supply
W2	5-V (V_{CC}), U1 analog supply

4 Circuit Board

This chapter shows the circuit board test points.

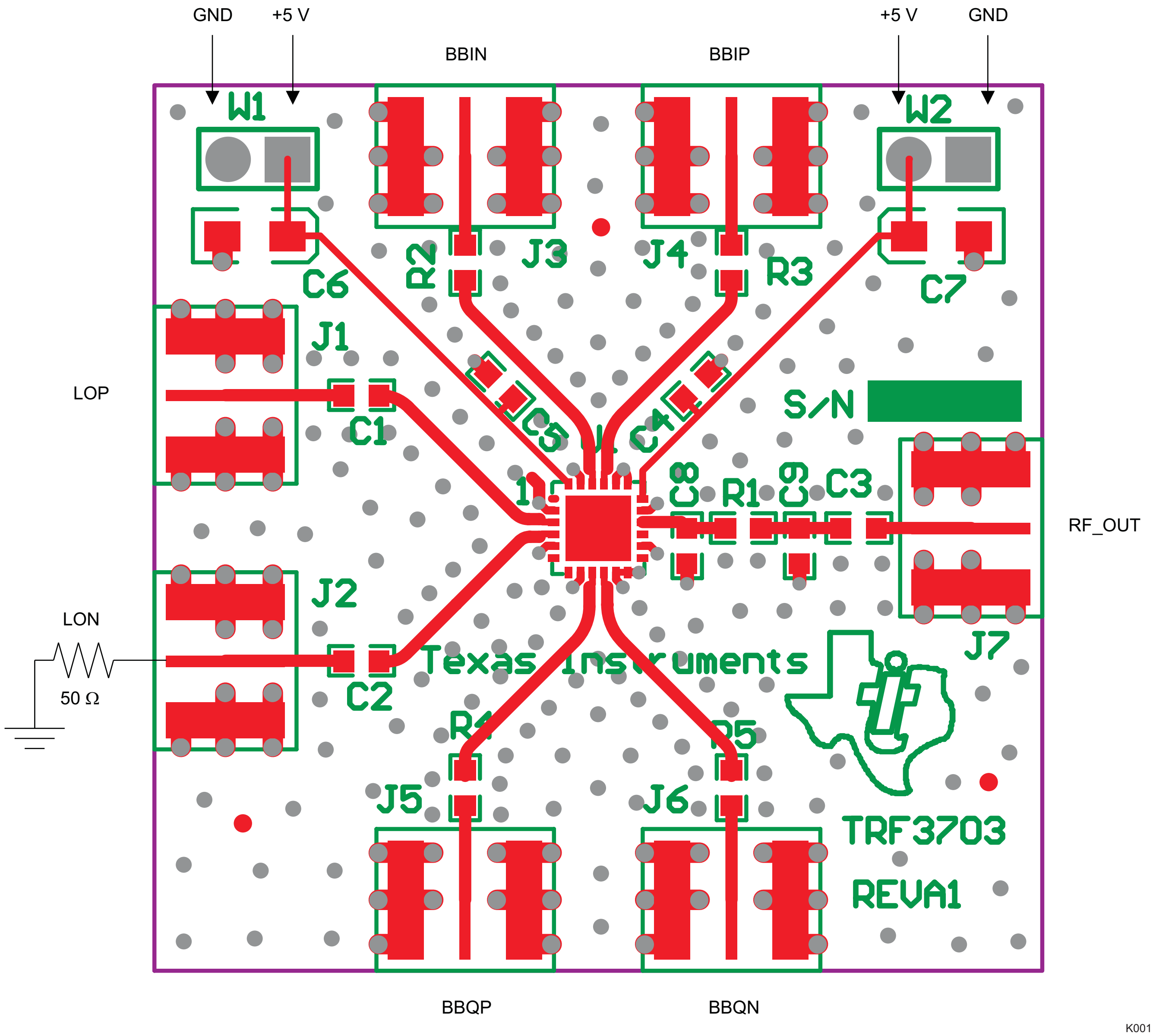
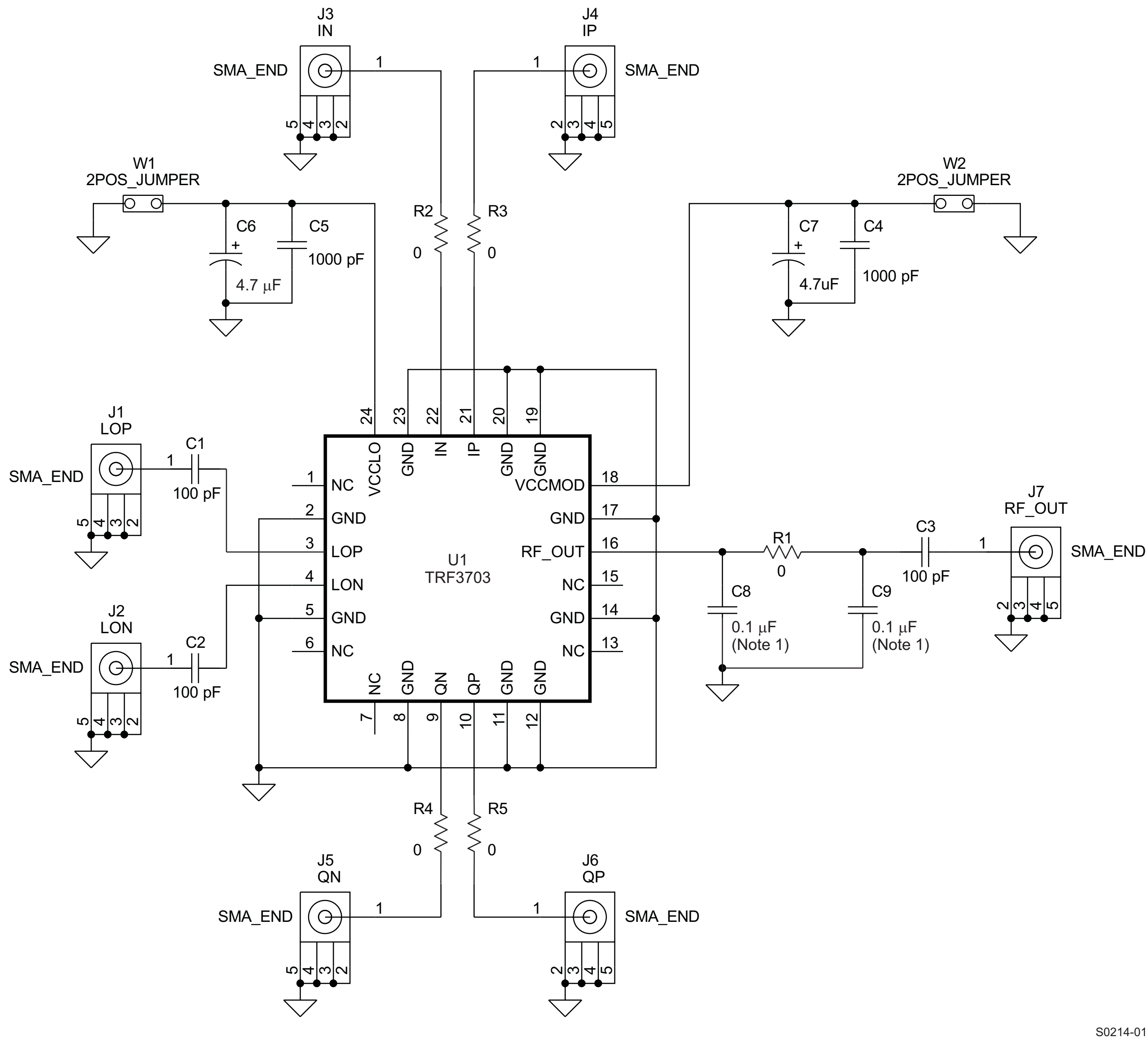


Figure 13. Silkscreen Top Layer

5 Schematic

This chapter shows the EVM schematic.



(1) Do not install.

Figure 14. TRF3703 EVM Schematic

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 4.5 V to 5.5 V and the output voltage range of 4.5 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 59°C. The EVM is designed to operate properly with certain components above –40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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